CLAIMS

1. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

    forming a first region and a second region of opposite conductivity type in the semiconductor layer, the first region and the second region being electrically isolated by an isolation region;

    forming a control electrode dielectric overlying the first region and the second region;

    forming a silicon-containing layer overlying and in contact with the control electrode dielectric;

    patterning a mask layer to overlie a selective portion of the silicon-containing layer;

    depositing a first metal layer overlying the silicon-containing layer and the mask layer;

    annealing the semiconductor device structure to form a first control electrode silicide by chemical reaction between the first metal layer and those portions of the silicon-containing layer not underlying the mask layer;

    removing remaining portions of the first metal layer that did not chemically react with the silicon-containing layer;

    removing the mask layer;

    depositing a second metal layer overlying the first control electrode silicide and the silicon-containing layer;

annealing the semiconductor device structure to form a second control electrode silicide by chemical reaction between the second metal layer and the silicon-containing layer;

removing remaining portions of the second metal layer that did not chemically react with the silicon-containing layer;

forming a conducting layer overlying the first control electrode silicide and the second control electrode silicide;

patterning the conducting layer, the first control electrode silicide and the second control electrode to form a first control electrode stack and a second control electrode stack having differing metal silicide content.

2. The method of claim 1 further comprising:

forming a first transistor with the first control electrode stack and forming a second transistor with the second control electrode stack.

3. The method of claim 1 further comprising selecting the first metal layer to comprise titanium, tantalum, platinum or tungsten to form the first control electrode silicide and having a predetermined work function value.

4. The method of claim 1 further comprising selecting the first metal layer to comprise a combination of two or more of titanium, tantalum, platinum or tungsten in a predetermined ratio to form the first control electrode silicide with varying composition.

5. The method of claim 1 further comprising selecting the first metal layer to have a first material overlying a second material, wherein the first material is substantially more immune to oxidation effects than the second material, thereby making the removing of remaining portions of the first metal layer easier after formation of any of the first control electrode silicide or the second control electrode silicide.

6. The method of claim 1 further comprising selecting the second metal layer to comprise molybdenum, chromium, hafnium or zirconium to form the second control electrode silicide having a predetermined work function value.

7. The method of claim 1 further comprising selecting the second metal layer to comprise a combination of two or more of molybdenum, chromium and zirconium in a predetermined ratio to form the second control electrode silicide with varying composition.

8. The method of claim 1 further comprising annealing the semiconductor device to form the first control electrode silicide at a first temperature that is substantially higher than a second temperature that is used to form the second control electrode silicide, thereby avoiding modifying electrical properties of the first control electrode silicide when the second control electrode silicide is being formed.

9. The method of claim 1 further comprising forming the semiconductor layer as either a silicon-containing substrate or a silicon-on-insulator substrate.

10. The method of claim 1 further comprising forming the conducting layer with in-situ doped polysilicon.

11. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first region and a second region of opposite conductivity type in the semiconductor layer, the first region and the second region being electrically isolated by an isolation region;

forming a control electrode dielectric overlying the first region and the second region;

forming a silicon-containing layer overlying and in contact with the control electrode dielectric;

patterning a mask layer to overlie a selective portion of the silicon-containing layer;

depositing a first metal layer overlying the silicon-containing layer and the mask layer;

annealing the semiconductor device structure to form a first control electrode silicide by chemical reaction between the first metal layer and those portions of the silicon-containing layer not underlying the mask layer;

removing remaining portions of the first metal layer that did not chemically react with the silicon-containing layer; and

exposing the semiconductor device in an oxygen rich environment to modify a thickness of a portion of the control electrode dielectric that is not underlying the first control electrode silicide.

12. The method of claim 11 further comprising:

depositing a second metal layer overlying the first control electrode silicide and the silicon-containing layer;

annealing the semiconductor device to form a second control electrode silicide from the silicon-containing layer; and

forming first and second transistor control electrode stacks respectively using the first control electrode silicide and the second control electrode silicide, the first and second transistor control electrode stacks having differing work functions.

13. The method of claim 11 further comprising:

depositing a conductive layer overlying the semiconductor device structure;

selectively patterning the semiconductor device structure for forming a first control electrode stack and a second control electrode stack respectively having first and second differing work functions; and forming first and second transistors having different control electrode dielectric thickness by respectively using the first control electrode stack and the second control electrode stack.

14. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first region and a second region of opposite conductivity type in the semiconductor layer, the first region and the second region being electrically isolated by an isolation region;

forming a control electrode dielectric overlying the first region and the second region;

forming a silicon-containing layer overlying and in contact with the control electrode dielectric;

patterning a mask layer to overlie a selective portion of the silicon-containing layer;

depositing a first metal layer overlying the silicon-containing layer and the mask layer;

annealing the semiconductor device structure to form a first control electrode silicide of a first control electrode by chemical reaction between the first metal layer and those portions of the silicon-containing layer not underlying the mask layer, the first control electrode silicide being formed without patterning the first metal layer;

removing remaining portions of the first metal layer that did not chemically react with the silicon-containing layer;

removing the mask layer;

forming a second control electrode having a different work function than the first control electrode; and

completing formation of a first transistor using the first control electrode and completing formation of a second transistor using the second control electrode.

15. The method of claim 14 further comprising:

exposing the semiconductor device structure in an oxygen rich environment prior to forming the second control electrode and completing formation of the first transistor and the second transistor, the oxygen rich environment modifying a thickness of a portion of the control electrode dielectric that is not underlying the first control electrode silicide.

16. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first region and a second region of opposite conductivity type in the semiconductor layer, the first region and the second region being electrically isolated by an isolation region;

forming a control electrode dielectric overlying the first region and the second region;

forming a silicon-containing layer overlying and in contact with the control electrode dielectric;

doping a first portion of the silicon-containing layer with a first predetermined dopant material;

doping a second portion of the silicon-containing layer with a second predetermined dopant material;

depositing a metal layer overlying the silicon-containing layer;

annealing the semiconductor device to form a first control electrode silicide in the first portion of the silicon-containing layer and to form a second control electrode silicide in the second portion of the silicon-containing layer;

forming a first control electrode from the first control electrode silicide and forming a second control electrode from the second control electrode silicide; and

completing formation of a first transistor using the first control electrode and completing formation of a second transistor using the second control electrode.

17. The method of claim 16 wherein the depositing of the metal layer further comprises:

selectively depositing a first metal layer overlying the first portion of the silicon-containing layer;

forming a first silicide control electrode by annealing the semiconductor device at a first temperature;

selectively depositing a second metal layer overlying the second portion of the silicon-containing layer; and

forming a second silicide control electrode by annealing the semiconductor device at a second temperature that is substantially lower than the first temperature;

wherein the first silicide control electrode has a different work function than the second silicide control electrode.

18. The method of claim 16 further comprising:

depositing the metal layer as a single metal layer overlying both the first portion and the second portion of the silicon-containing layer.

19. The method of claim 16 further comprising:

exposing the semiconductor device structure in an oxygen rich environment prior to forming the second control electrode silicide, the oxygen rich environment modifying a thickness of a portion of the control electrode dielectric that is not underlying the first control electrode silicide.

20. The method of claim 16 further comprising:

depositing in-situ doped polysilicon overlying the first control electrode silicide and the second control electrode silicide for use as part of the first control electrode and the second control electrode.